

1,

Memory Location

20	LOAD	50
21	ADD	51
50	724	
51	006	

(a) at the conclusion of instruction at location 20 LOAD 50

(IR) = 550

(MAR) = 50

(MDR) = 724

(PC) = 21

(b) show the contents of each register as each step of the fetch-execute cycle is performed for instruction

21 ADD 51

Micro-operation	PC	MAR	MDR	A	IR
Fetch instruction					
MAR ← PC	21	21	724	724	550
MDR ← memory	21	21	151	724	550
IR ← MDR	21	21	151	724	151
Execute instruction					
MAR ← IR	21	51	151	724	151
MDR ← memory	21	51	006	724	151
A ← A + MDR	21	51	006	730	151
PC ← PC + 1	22	51	006	730	151

2,

$$2^{36} = 1\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000$$

the address range is from 0000 0000 0000 0000 0000 0000 0000 0000 0000
to 1111 1111 1111 1111 1111 1111 1111 1111 1111

3,

for both (a) and (b)

the maximal memory address is 2^{16} , it is 1111 1111 1111 1111 in binary notation,

the difference between (a) and (b) is only the size of a word corresponding to each memory cell, one is 16 bits each, the other is 8 bits each. While the address ability is still 16 bits, the capability to access the total number of the memory cells is the same.

4,

the following is of binary notation

(a) by shift two bits to the left, the result equals to the product when it is multiplied by 2^2 , if it does not overflow. by shift one bit to the right, the result equals to the Quotient when it is divided by 2^1 ;

Shifting an unsigned number two bits to the left multiplies it by four, unless the value overflows. Overflow occurs if either of the two leftmost bits is a 1.

(b) Any mix of 1's and 0's in the three leftmost bits will cause an overflow, and possibly a sign change as well. If all three leftmost bits are the same, the value is algebraically quadrupled.

(c) The left shift still requires the leftmost bits to be the same, otherwise overflow occurs. However, at least the sign is now correct. Right shifts will divide the value in half for each bit shifted, provided that the sign bit is carried to the right each time. This assures a succession of 1's or 0's at the leftmost bit positions, and preserves the sign.

5,

$$\text{Bus_cycle} = 4 * \text{Clock_cycle} = \frac{4}{8\text{MHz}}$$

2 Bytes transferred every Bus cycle, thus the transfer rate is $\frac{2}{4/8\text{MHz}} = 4\text{MBytes/sec}$

6,

The clock cycle and the instruction execution time are important metrics to measure the computer speed. But it is still hard to say. I/O access, memory access, even different operating system will affect the overall performance. Usually, different computers suit their own kinds of tasks.

Usually we use a series of standard test packages as benchmark to evaluate the computer speed.

7,

There are two different registers associated with memory because each memory location has an address that identifies it and the data that is stored there, just as each mailbox in the LMC has both an address and the slip of paper containing the data stuffed into the slot.

MAR hold the address, MDR accept the content read from the memory indicated by the MAR.

8,

To fully harness the hardware resource, the address capacity 268, 435, 456 can be covered exactly by 28 bits of address register or 28 bits of address bus.

(268,435,456=1 0000 0000 0000 0000 0000 0000 in binary format),

Therefore, the memory address range is from 0000 0000 0000 0000 0000 0000 0000 to 1111 1111 1111 1111 1111 1111 1111