SCHOOL OF COMPUTER SCIENCE AND INFORMATION TECHNOLOGY

G51CSA

Third (last) Homework

Deadline: Friday, 6th December 2002. Before 10:00 class, LT2

1. Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

   (a) How many total bytes of memory can be stored in cache?
   (b) How is a 16-bit memory address divided into tag, line number, and byte number?
   (c) Into which line would bytes with each of the following addresses be stored?

   0001 0001 0001 1011
   1100 0011 0011 0100
   1101 0000 0001 1101
   1010 1010 1010 1010

   (d) Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

2. A disk has as specification as: 512 byte/sector, 96 sector/track, 110 track/surface, 8 usable surfaces, and rotation speed 360 rpm. A processor reads one sector from the disk use interrupt driven I/O, with one interrupt per byte. If it take 2.5 *m*s to process each interrupt, what percentage of time will the processor handling I/O (disregard seek time and latency time).

3. The following sequence of virtual page number is encountered in the course of execution on a computer with virtual memory:

   3, 4, 2, 6, 7, 1, 3, 2, 6, 3, 5, 1, 2, 3

   Assume that least recently used (LRU) page replacement policy is adopted. Plot a graph of page hit rate (fraction of page references in which the page is in main memory) as a function of main memory page capacity n for $1 \leq n \leq 8$. Assume that main memory is initially empty.