SCHOOL OF COMPUTER SCIENCE AND INFORMATION TECHNOLOGY

G51CSA Homework/Tutorial Problems – #3

The following problems are adopted from reference C, Irv Englander, **The architecture of Computer Hardware and Software**, John Wiley & Sons, Inc, 2000, pp. 199

1. Suppose that the following instructions are found at the given location of the memory:

Memory Location	Instruction	Description
20	LOAD 50	;load data into accumulator from location 50
21	ADD 51	;add data in location 51 and accumulation and save the result in Accumulator
50	724	;Data
51	006	;Data

   (a) show the contents of the IR, the PC, the MAR, the MDR and A (accumulator) at the conclusion of instruction 20
   (b) show the contents of each register as each step of the fetch – execute cycle is performed for instruction 21

2. One large modern computer has a 36-bit memory address register. How much memory can this computer address? (i.e., how many memory locations can this computer address)

3. Consider a hypothetical microprocessor generating a 16 bit address (for example assume that both the program counter and the address register are 16-bit wide) and having a 16-bit data bus.

   (a) What is the maximum memory address space that the processor can access directly if it is connected to a “16-bit memory" (i.e., each memory location holds 16 bits)
   (b) What is the maximum memory address space that the processor can access directly if it is connected to a “8-bit memory" (i.e., each memory location holds 8 bits)

4.
   (a) What is the effect of shifting an unsigned number in a register two bits to the left? One bit to the right? Assume that 0’s are inserted to replace bit locations at the end of the register that have become empty due to shift
   (b) Suppose that number is signed, that is, stored using 2’s complement. Now what is the effect of shifting the number
   (c) Suppose that the shift excludes the sign bit, so that the sign bit always remains the same. Furthermore, suppose that during a right shift, the sign bit is always used as the insertion bit at the left end of the number (instead of 0). Now what is the effect of these shifts?

5. Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equal to four input clock cycles. What is the maximum data transfer rate (bits per second) that this microprocessor can sustain? To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? State any other assumption you make, and explain. ((Main text, William Stallings, p 91)

6. On computer A, all instructions take 10 nsec to execute. On computer B, they all take m nsec to execute. Can you say for certain that computer B is faster? Discuss (Reference B, p113)

7. Why are there two different registers (MAR and MDR) associated with memory? What are the equivalents in the Little Man Computer? (Reference C p. 199)

8. A certain computer can be equipped with 268,435,456 byes of memory. Why would a manufacturer choose such a peculiar number, instead of an easy to remember one like 250,000,000? (Reference B, p. 115)